

# A Novel Grid-based Algorithm for Decoder Routing in Semiconductor Design

Hong-Yeon Kim, Jeongsun Ahn, Chae-Young Kim and Hyun-Jung Kim

**Abstract**— Decoders which convert  $n$  bits of binary information into up to  $2^n$  outputs in the semiconductor memory device to generate decoded data usually have a rectangular shape with one side longer to selectively control a large number of output signals. When designing a decoder layout, design rules, such as the width rule, spacing rule, and enclosure rule, vary depending on the purpose of the semiconductor device or process technology, but there are several rules that are generally observed. In this study, the routing problem which connects input and output terminals is addressed in a novel grid environment designed by reflecting those basic design rules. The objective is to minimize the total length and the number of bending points, and the A\* algorithm is applied to a newly designed grid environment.

**Keywords:** Circuit routing, Design rule, Semiconductor chip, Decoder layout

## I. INTRODUCTION

As Moore’s Law reaches its limit, the pressure is mounting to improve semiconductor performance by putting more transistors in a limited space [1]. In particular, the growth of portable digital devices and the emergence of packaging technology that places memory and non-memory semiconductors together accelerates the slim layout of semiconductors [2]. In the memory semiconductor, a decoder determines whether to store data by adjusting the open/close of the transistor. Decoders which control a large number of output signals with a relatively small number of input signals typically have a rectangular shape with one side longer along with the array of the output terminals (also called nodes). There are several rules, called design rule checking (DRC) rules, that must be followed in a decoder layout to function properly and keep consistent performance of the decoder. In addition to DRC rules, some electrical properties, such as routing width or the number of bends also affect the quality of a decoder. A routing problem which adds (metal) wires needed to connect pairs of I/O terminals at the shortest distance while adhering to these special restrictions is known to be an NP-complete problem [3]. We provide an efficient heuristic algorithm for the routing problem by designing a novel grid environment.

## II. PROBLEM DEFINITION

When designing a decoder layout, design rules vary depending on the purpose of the semiconductor or process technology, but there are several rules that are generally observed [4]. The first rule is a width rule, illustrated in Fig. 1(a), which enforces the minimum width of a wire in a routing path for smoothly transmitting current. The second rule is a spacing rule, in Fig. 1(b), which requires a

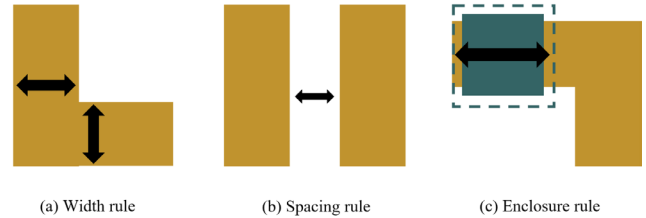


Figure 1. Basic layout design rules.

minimum distance between two adjacent wires to avoid current confusion and performance degradation of the semiconductor. The third rule is an enclosure rule, illustrated in Fig. 1(c), which represents the minimum area that the metal wire should occupy relative to the terminal center. In this study, routing paths which connect given pairs of I/O terminals are found while satisfying these three basic rules. The objective is to minimize the total distance of wires used for connecting all pairs of I/O terminals and the number of bending points in the paths. Minimizing the number of bending points allows the efficient use of a limited routing area and reduces the resistance of circuits. Also, the wires cannot be overlapped. We use the A\* algorithm by designing a new cost function in a novel grid environment.

## III. DESIGN RULE-BASED GRID ENVIRONMENT

Most previous studies have conducted global routing, which approximately determines the path direction and bending points, and then detailed routing, which fixes the actual coordinates of the paths [5]. DRC rules are mainly considered in the detailed routing, and if there is no feasible solution, a global routing process is repeated. We propose a novel approach which combines the global and detailed routing by designing a new grid environment where the size of cells is determined by considering DRC rules. The decoder layout has a rectangular shape due to the nature of having more output nodes than input nodes. We define a channel as the number of cells that can fit in a routing area while satisfying the DRC rules. One cell in a grid environment represents a unit path which must satisfy the width and spacing rules. At the same time, it also needs to be as small as possible to use a limited area efficiently. When the minimum width and the minimum space are denoted as  $\omega$  and  $\lambda$ , respectively, the cell size is determined by  $\omega + \lambda$  obtained from adding two  $\lambda/2$  to  $\omega$  as illustrated in Fig. 2(a). According to the enclosure rule, the node should be covered with a metal wire having some margin as much as  $\gamma$ . There also exists a spacing rule between the covered metal wire and the other routing wire. Therefore, the cell where the node is located becomes a square with the size  $\gamma + \lambda$ , and the cells on the same row are designed as a rectangular with a height of  $\gamma + \lambda$  and a width of  $\omega + \lambda$  as illustrated in Figs. 2(b) and (c).

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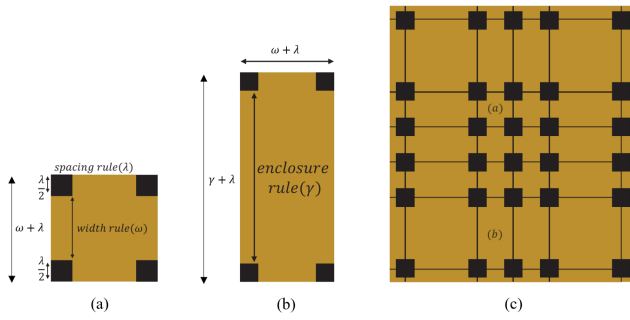


Figure 2. Transformed grid environment.

#### IV. A\* ROUTING ALGORITHM

The A\* algorithm can provide a shortest path between a pair of nodes [6]. However, it does not consider the subsequent paths that need to be added to connect other pairs of nodes. Fig. 3(a) shows an example where multiple bending points occur with the A\* algorithm building a path from the green to red cells. Such a path derived from the simple A\* algorithm significantly reduces the space used by other paths as indicated with the red box in Fig. 3(a). Also, many bending points increase the resistance and the probability of errors in the subsequent patterning process [7]. Therefore, it is necessary to derive a path that avoids encroaching on a specific area as much as possible while reducing the number of bending points. Fig. 3(b) shows a path which minimizes the number of bending points and also the distance but still uses the large portion of the red box. Fig. 3(c) shows another path which avoids using the space in the red box while the number of bending points is larger than that in Fig. 3(b). In practice, the path in Fig. 3(c) is preferred because other wires can be added while satisfying complicated design rules. We therefore design a cost function of the A\* algorithm by considering the number of bending points included in the candidate path and the preferred direction which has less impact on the channel. Fig. 4 shows a simple but practical decoder routing example obtained by using the bend and preferred direction cost in the A\* algorithm.

#### V. CONCLUSION

We have proposed a novel grid design and a cost function of the A\* algorithm for the decoder routing. The proposed approach can combine the global and detailed routing and provide a feasible and efficient solution in a short time. Better performance could be reached if node pairing specific to this routing is studied.

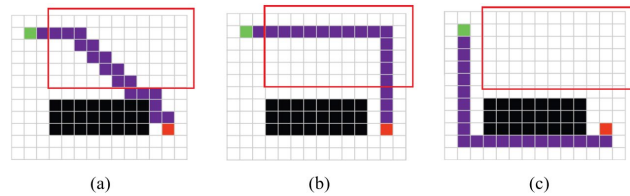


Figure 3. A\* algorithm path finding with heuristic cost.

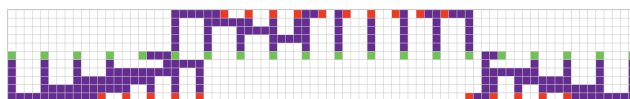


Figure 4. A decoder routing example.

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